a leveling film covering each of said thin film transistors in both of the pixel portion and a part of the driver circuit portion,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

22. (Amended) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor. each of said transistors comprising:

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a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the shift register,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

23. (Amended) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

24. (Amended) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

25. (Amended) An active matrix display device having a pixel portion and a driver circuit portion, said driver circuit portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

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a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and a part of the driver circuit portion,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

26. (Amended) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and in the shift register,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

27. (Amended) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 cm2/V·sec or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 cm2/V·sec or more, and

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

28. (Amended) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

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a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 cm^2/V·sec or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 cm^2/V·sec or more,

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

29. (Amended) An active matrix display device having a pixel portion and a driver circuit portion, said driver circuit portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said p-channel and n-channel thin film transistors in both of the pixel portion and a part of the driver circuit portion,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more,

wherein each of said semiconductor islands has a thickness in the range of ~~5000~~ Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than 7×10^{19} cm^{-3}.

30. (Amended) A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the shift register,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more,

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

31. (Amended) A semiconductor circuit having a pixel portion and an inverter, said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

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a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V \cdot sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V \cdot sec$ or more,

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

32. (Amended) A semiconductor circuit having a pixel portion and a clocked inverter, said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region;

a gate electrode adjacent to said gate insulating film; and

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V{\cdot}sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V{\cdot}sec$ or more,

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less, and

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

41. (Amended) An active matrix display device including a pixel portion and a driver circuit portion comprising:

a plurality of pixel electrodes formed on an insulating surface;

a first plurality of thin film transistors being formed in the pixel portion on said insulating surface and being connected to said pixel electrodes;

a second plurality of thin film transistors being formed in the driver circuit portion on said insulating surface, said second plurality of thin film transistors including at least one pair of complementary p-channel and n-channel thin film transistors; and

a leveling film covering both of the first and second plurality of thin film transistors in the pixel portion and a part of the driver circuit portion,

wherein said second plurality of thin film transistors in said driver circuit include channel semiconductor layers having at least one of an electron mobility 15 $cm^2/V \cdot sec$ or more and a hole mobility of 10 $cm^2/V \cdot sec$ or more, and

wherein each of said channel semiconductor layers has a thickness of 5000 Å or less.

Please add new claims 67-78 as follows.

--67. A device according to claim 22 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3}.

68. A device according to claim 23 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3}.

69. A device according to claim 24 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3}.

70. A device according to claim 25 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially same the as an absolute value of a threshold voltage of said p-channel thin film transistor.

71. A device according to claim 26 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially same the as an absolute value of a threshold voltage of said p-channel thin film transistor.

72. A device according to claim 27 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially same the as an absolute value of a threshold voltage of said p-channel thin film transistor.

73. A device according to claim 28 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially same the as an absolute value of a threshold voltage of said p-channel thin film transistor.

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74. A device according to claim 29 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3}.

75. A device according to claim 30 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3}.

76. A device according to claim 31 wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3}.